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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LAM, NELSON C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,949	AURACHER ET AL.	
	Examiner	Art Unit	
	Nelson Lam	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/24/2005*. 12/01/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication of 12/01/2003. Application 10/724,949 has been examined. In the examination of 10/724,949, claims 1-28 are pending.

Claim Objections

2. Claim 26 is objected to because of the following informalities: Claim 26 is a Markush claim therefore the claimed limitations need to be separated with a comma instead of a semicolon. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the **first** paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. **Claims 10-27 are rejected under 35 U.S.C. 112, first paragraph**, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. As to claim 10, in the specification the applicant does not support or define the meaning of the term "used sub-circuit cell". As to claim 15, in the specification the applicant does not support or define the meaning of the term "locally usable resources".

Claims 11-14 depend from rejected claim 10 and include all of the limitations of claim 10 thereby rendering these dependent claims indefinite. Claims 16-27 depend from rejected claim 15 and include all of the limitations of claim 15 thereby rendering these dependent claims indefinite.

5. The following is a quotation of the **second** paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 10-14 recites the limitation "used sub-circuit cell". There is insufficient antecedent basis for this limitation in the claim.

6. **Claims 15-27 are rejected under 35 U.S.C. 112, second paragraph**, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 15, the term "locally usable sources" is undefined. As per claim 18, the term "circuit arrays" is undefined.

Regarding claim 25, the claim is confusing based on the applicant's specification that the general purpose circuit elements typically comprise, for example, logic gates (e.g., NOR gates, etc.). Therefore, it is unclear how the general-purpose logic circuits are more complicated than the general purpose circuit elements.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. **Claims 1-21 and 27-28 are rejected under 35 U.S.C. 102(b)** as being anticipated by Vasishta et al. U.S. Patent No. 6,823,499.

As per **claim 1**, Vasishta discloses an integrated circuit comprising:

a die having a surface (Fig. 2A; col. 1, line 49-52; col. 3, line 65-66);

a first area of first circuit cells in said die configurable by user defined interconnections from above said surface (Abstract; Fig. 2A, #100, #110, #112; col. 2, line 51-54; col. 4, line 1-4; col. 6, line 1-5);

a second area comprising a plurality of sub-circuit cells forming a module having a predefined functionality, wherein said sub-circuit cells include at least one second circuit cell configured such that when said predefined functionality of said module is not used, said second circuit cell is configurable by user defined interconnections from above said surface (Abstract; Fig. 2A, #100, #102, # 104; col. 2, line 44-51; col. 4, line 1-6).

As per **claim 2**, Vasishta discloses the integrated circuit of claim 1, wherein said second circuit cell comprises at least one of a buffer circuit cell, an inverter circuit cell, a flip-flop circuit cell, a latch circuit cell, and an OR gate circuit cell (Fig. 3, #54; col. 5, line 21-24).

As per **claim 3**, Vasishta discloses the integrated circuit of claim 1, wherein said sub-circuit cells comprise a plurality of said second circuit cells (Fig. 3, #54; col. 5, line 21-24).

As per **claim 4**, Vasishta discloses the integrated circuit of claim 3, wherein said plurality of second circuit cells comprises a plurality of different circuit cell types (Fig. 3, #54; col. 5, line 21-24).

As per **claim 5**, Vasishta discloses the integrated circuit of claim 1, wherein each of said first circuit cells comprises an input terminal at said surface and an output terminal at said surface (col. 3, line 53-57; col. 4, line 45-52).

As per **claim 6**, Vasishta discloses the integrated circuit of claim 1, wherein said at least one second circuit cell comprises a first input terminal at said surface and a first output terminal at said surface (col. 3, line 53-57; col. 4, line 45-52).

As per **claim 7**, Vasishta discloses the integrated circuit of claim 6, further comprising:

at least one layer of conductive interconnections formed on said surface (Fig. 2B; col. 5, line 1-11);

wherein said first input terminal is coupled by a respective conductive interconnection in said layer to a stable signal line (Fig. 3; Fig. 4; col. 5, line 34-48; col. 6, line 14-20).

As per **claim 8**, Vasishta discloses the integrated circuit of claim 7, wherein said stable signal line is a stable voltage line (col. 5, line 45-48).

As per **claim 9**, Vasishta discloses the integrated circuit of claim 8, wherein said stable voltage line is a power rail (col. 5, line 45-48).

As per **claim 10**, Vasishta discloses the integrated circuit of claim 7, further comprising at least one used sub-circuit cell disposed among said unused circuit cells (col. 4, line 23-26, where sub-circuit cell are functional modules).

As per **claim 11**, Vasishta discloses the integrated circuit of claim 10, wherein said used sub-circuit cell comprises a second input terminal at said surface and a second output terminal at said surface (col. 4, line 23-26, where sub-circuit cell are functional modules; col. 3, line 53-57; col. 4, line 45-52).

As per **claim 12**, Vasishta discloses the integrated circuit of claim 10, wherein said used sub-circuit cell is configured as a repeater cell in a routing connection across said area (Fig. 3; col. 5, line 20-24, where gate is a repeater cell).

As per **claim 13**, Vasishta discloses the integrated circuit of claim 12, wherein said routing connection comprises (i) a first interconnection extending in said layer across a first portion of said area to said second input terminal, and (ii) a second interconnection extending in said layer across a second portion of said area from said second output terminal (Fig. 2A, #102, #106, #112; col. 4, line 22-40).

As per **claim 14**, Vasishta discloses the integrated circuit of claim 12, wherein said used sub-circuit cell comprises at least one of a buffer cell and an inverter cell (Fig. 1; col. 3, line45-49; col. 5, line 22-23, wherein a buffer cell and an inverter cell are logic gates).

As per **claim 15**, Vasishta discloses an integrated circuit comprising:

a die having a surface (Fig. 2A; col. 49-52; col. 3, line 65-66);

a first general purpose area of said die containing general purpose circuit elements configurable by user defined interconnections from above said surface (Abstract; Fig. 2A, #100, #110, #112; col. 2, line 51-54; col. 4, line 1-4; col. 6, line 1-5); and

a plurality of second standard circuit areas containing standard sub-circuits more complicated than said general purpose circuit elements and configurable by user defined interconnections from above said surface (Fig. 3, #44, #46, #48, #50, #52, #54; col. 5, line 12-24);

wherein said plurality of second standard circuit areas are distributed across aid first general purpose area at multiple locations and provide locally usable resources at said multiple locations in said first general purpose area (Fig. 3, #54; col. 5, line 22-24).

As per **claim 16**, Vasishta discloses the integrated circuit of claim 15, wherein said plurality of second standard circuit areas are distributed in a substantially uniform pattern (Fig. 3, #54; col. 5, line 21-24; col. 4, line 53-58, where uniform pattern is interpreted as being an array).

As per **claim 17**, Vasishta discloses the integrated circuit of claim 15, wherein said plurality of second standard circuit areas are distributed according to a repeating pattern (Fig. 3, #54; col. 5, line 21-24; col. 4, line 53-58, where repeating pattern is interpreted as being an array).

As per **claim 18**, Vasishta discloses the integrated circuit of claim 15, wherein said plurality of second standard circuit areas comprise a plurality of circuit arrays (Fig. 3, #54; col. 5, line 21-24; col. 4, line 53-58).

As per **claim 19**, Vasishta discloses the integrated circuit of claim 15, wherein said general purpose circuit elements comprise logic circuits (Fig. 3, #54; col. 5, line 21-24).

As per **claim 20**, Vasishta discloses the integrated circuit of claim 15, wherein said general purpose circuit elements comprise one or more logic gates (Fig. 3, #54; col. 5, line 21-24).

As per **claim 21**, Vasishta discloses the integrated circuit of claim 15, wherein said standard sub-circuits comprise logic circuits (Fig. 3, #54; col. 5, line 21-24).

As per **claim 27**, Vasishta discloses the integrated circuit of claim 15, further comprising:

at least one layer of conductive interconnections formed on said surface (Fig. 2B; col. 5, line 1-11);

wherein (i) said general purpose circuit elements are coupled to said conductive interconnections in said at least one layer (Fig. 4; col. 6, line 12-17), and (ii) said standard sub-circuits are coupled to said conductive interconnections in said at least one layer (Fig. 4; col. 6, line 12-17; col. 6, line 24-29).

As per **claim 28**, Vasishta discloses a method for designing an integrated circuit element, comprising the steps of:

(a) providing a first area of said integrated circuit element comprising first circuit cells configurable by user defined interconnections above a surface of said integrated circuit element (Abstract; Fig. 2A, #100, #110, #112; col. 2, line 51-54; col. 4, line 1-4; col. 6, line 1-5); and

(b) providing a second area of said integrated circuit element comprising a plurality of sub-circuit cells forming a module having a predefined functionality, wherein said sub-circuit cells include at least one second circuit cell configured such that when said predefined functionality of said module is not used, said second circuit cell is configurable by user defined interconnections from above said surface (Abstract; Fig. 2A, #100, #102, # 104; col. 2, line 44-51; col. 4, line 1-6).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vasishta in view of Actel Introduction to Actel FPGA Architecture (Actel Application Note). Vasishta discloses all the limitations of claim 15 referred above. Vasishta does not explicitly disclose the use of a buffer array cell but discloses a single logic element, such as a gate (Vasishta: col. 5, line 22-23). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made that the I/O buffers shown in Fig. 1 are analogous to the claimed buffer array circuit cells.

As per **claim 22**, Actel Application Note discloses the integrated circuit of claim 15, wherein said standard sub-circuits comprise a first buffer array circuit cell. (Fig. 1, Fig. 8). I/O buffers as shown by the various configuration illustrated in the Actel Application Note are by definition buffer array circuit cells.

As per **claim 23**, Actel Application Note discloses the integrated circuit of claim 22, wherein said first buffer array circuit cell comprises an array of buffer circuits, wherein (i) each buffer circuit comprises an input terminal and an output terminal (Fig. 8, Fig. 9), and (ii) adjacent buffer circuits are oppositely orientated (Fig. 8, Fig. 9).

As per **claim 24**, Actel Application Note discloses the integrated circuit of claim 22 wherein said standard sub-circuits further comprise a second buffer array circuit cell

extending in a different physical direction from said first buffer array circuit cell (Fig. 1, where the I/O buffers are shown in both horizontal and vertical directions).

As per **claim 25**, Actel Application Note discloses the integrated circuit of claim 24, wherein said standard sub-circuits further comprise general purpose logic circuits more complicated than said general purpose circuit elements (Fig. 1 illustrates I/O buffer logic circuits).

As per **claim 26**, Actel Application Note discloses the integrated circuit of claim 25, wherein said general purpose logic circuits comprise at least one of:

an individual buffer (Fig. 8 illustrates an individual buffer), a logic gate different from said general purpose circuit elements, a multiplexer (Fig. 4 illustrates a multiplexer), and a flip flop (Fig. 6; Fig. 7; Fig. 9; Fig. 10, all illustrate a D-type flip flop).

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson Lam whose telephone number is 571 272-8318. The examiner can normally be reached on 9am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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